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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,694	12/11/2003	David W. Boerstler	ROC920030116US1	8664
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IBM CORPORATION			NGUYEN, HAIL	
ROCHESTER IP LAW DEPT. 917				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/733,694	BOERSTLER ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	HAI L. NGUYEN	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 02 January 2008.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-3 and 5-17 is/are rejected.  
 7) Claim(s) 4 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 02 January 2008 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____.   | 6) <input type="checkbox"/> Other: _____ .                        |

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment received on 01/02/2008 has been reviewed and considered with the following results:

As to the rejection to claims 10-15 and 17, under 35 U.S.C. 112, 1st paragraph, Applicant's clarifications of the claims have been carefully reviewed, but are not persuasive. Since, the claimed function must be supported by the drawings. Therefore, the rejections are maintained as set forth below.

As to the rejections to claims 4 and 9-15, under 35 U.S.C. 112, 2nd paragraph, Applicant's amendments and newly amended drawings have overcome the rejections, as such; the rejections have been withdrawn.

As to the prior art rejections to claims 1-3, 5-9 and 16, the arguments by the Applicant have been carefully reviewed but are not persuasive because the claimed limitations as clearly anticipated by the cited reference. Examiner's response to Applicant's arguments for supporting the prior art rejections are addressed in detail below.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 10-15 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed limitations that “determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state”, in claim 10. The details of such claimed functions are not seen in the description of the preferred embodiment. Therefore, it is not clear as currently defined, how the circuits can perform those recited functions as recited in claim 10. Furthermore, claim 17 is similarly rejected; note the above discussion with regard to claim 10.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5-9 and 16 are rejected under 35 U.S.C 102(e) as being anticipated by Nguyen (US 6,600,355).

With regard to claims 1 and 8, Nguyen discloses in Figs. 2-3A a multiplexer system, and a method of use thereof, comprising a multiplexer (202) having a plurality of data input nodes adapted to receive a plurality of input signals (CLK0, CLK90, CLK180, CLK270); an output node (CKOUT) adapted to selectively output one of the plurality of input signals; a plurality of select nodes (S0, S90, S180, S270), each select node corresponding to a different one of the

plurality of data input nodes and adapted to cause the multiplexer to select a different one of the plurality of input signals for output by the output node in response to a select signal of a first logic state being provided to the select node; and selection circuitry (201) coupled to the multiplexer and adapted to prevent a first of the select signals that is in the first logic state (logic High) from being provided to the multiplexer until the other select signals are in a second logic state (logic Low).

With regard to claims 2 and 9, the plurality of input signals comprises a plurality of clock signals (CLK0, CLK90, CLK180, CLK270).

With regard to claim 3, wherein the plurality of clock signals are asynchronous relative to one another (as depicted in Fig. 3A).

With regard to claim 5, the method further comprises a step of synchronizing the first (S0) of the select signals with a corresponding first (CLK0) of the input signals of the multiplexer prior to providing the first of the select signals to the multiplexer (as depicted in Fig. 3).

With regard to claim 6, wherein synchronizing the first (S0) of the select signals comprises preventing the first (CLK0) of the select signals from reaching the multiplexer until after a rising edge and a falling edge of the first of the input signals (as depicted in Fig. 3A).

With regard to claims 7 and 16, Nguyen discloses in Figs. 2-3A a multiplexer system, and a method of use thereof, comprising a multiplexer (202) having a plurality of data input nodes adapted to receive a plurality of input signals (CLK0, CLK90, CLK180, CLK270); an output node (CKOUT) adapted to selectively output one of the plurality of input signals; and a plurality of select nodes, each select node corresponding to a different one of the plurality of data input

nodes and adapted to cause the multiplexer to select a different one of the plurality of input signals for output by the output node in response to a select signal of a first logic state being provided to the select node; and selection circuitry (201) coupled to the multiplexer and adapted to: prevent a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state; and prevent the first of the select signals from reaching the multiplexer until after a rising edge and a falling edge of a corresponding first (CLK0) of the input signals of the multiplexer (see Fig. 3).

### ***Response to Arguments***

6. In response to Applicants' arguments regarding to 10-15 and 17, which is rejected under 35 U.S.C. § 112, 1st paragraph, Applicants point to the corresponding text (page 6, line 14 through page 7, line 15) of the specification and in conjunction with newly amended drawings (Fig. 2), as supporting/enabling the recitations of the claim. However, Examiner respectfully disagree because none of them can be seen as supporting/enabling the recitations of the claims for at least the following reasons. For example, when only the select signal E1 is in the first logic state (in logic state high as described in the specification), and the others are in a second logic state (in logic state low as described in the specification). That causes NAND gate 206a and the latches outputting a logic state low output; which will cause other select signals E2-E4 passed through other NAND gates and latches because all of select signals (C1-C4 of NAND gates 206b-206d) as described in the disclosure (page 6, line 14 through page 7, line 1). Therefore, there is nothing in the disclosure as supporting/enabling the claimed functions as "determine if only one of the input select signals is in the first logic state, and if so, output at

least the select signal that is in the first logic state". As discussed above, Examiner do not find any part of the cited text of the specification and the accompanying drawings as supporting/enabling the recitations of the claims. Therefore, the rejections to claims 10-15 and 17 are proper and remain.

7. In response to Applicants' arguments regarding to claims 1-3, 5-9 and 16, which are rejected under 35 U.S.C. § 102(e), Applicants state that "the select signals output by the state machine of Nguyen are provided to the multiplexer, as are the clock signals, but there is no prevention of a first of the select signals in a first logic state from being provided to the multiplexer until all other select signals are in a second logic state", as in claim 1, is not persuasive. As discussed above, for example, Nguyen clearly teaches a multiplexer system (as shown in Fig. 2) comprising a selection circuitry (201) which only provides one of the select signals, i.e. the select signal S270, is in the first logic state (High) while other select signals, i.e. the select signals S0, S90 and S180, are in the second logic state (Low). Similar responses apply to claims 7, 8, 16, and 17. Therefore, the claimed limitation "preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state" is clearly anticipated by the reference. Therefore, the rejections of record are still believed to be proper and are therefore maintained as set forth above.

#### ***Allowable Subject Matter***

8. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a method for multiplexing signals, as recited in claim 4, having a very specific structural limitation such as a step of preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state comprises the steps of performing a NOR operation on the other select signals to generate a NOR output; and performing a NAND operation on the first of the select signals and the NOR output, and being configured in combination with the rest of the limitations of the base claim 1.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and

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Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. L. N./  
Examiner, Art Unit 2816  
March 29, 2008

/N. Drew Richards/  
Supervisory Patent Examiner, Art Unit 2816